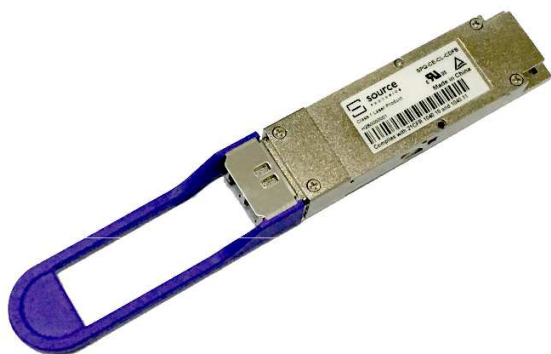




Features

- Compliant with QSFP28 Standard: SFF-8665 Revision 1.9, SFF-8636 Revision 2.7
- Compliant with 4WDM-10 MSA Revision 1.0
- High speed I/O electrical interface (CAUI-4)
- Single 3.3V Supply Voltage
- Maximum power consumption 3.5W
- 0-70 °C Case Operating Temperature
- CWDM DML laser and PIN Receiver Array
- QSFP28 MSA package with duplex LC connector
- Two Wire Serial Interface with Digital Diagnostic Monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

Absolute Maximum Ratings

Table 1 – Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_s	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.3	-	3.6	V	
Relative Humidity (non-condensing)	RH	5	-	95	%	
Data Input Voltage – Differential	$IV_{DIP}-V_{DIN}$	-	-	1.0	V	
Control Input Voltage	V_I	-0.3	-	$V_{CC}+0.5$	V	
Control Output Current	I_O	-20	-	20	mA	

Recommended Operating Conditions

Table 2 – Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	-	70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I_{CC_IP}	-	-	1400	mA	
Sustained peak current at hot plug	I_{CC_SP}	-	-	1155	mA	
Maximum Power Dissipation	P_D	-	-	3.5	W	
Maximum Power Dissipation, Low Power Mode	P_{DLP}	-	-	1.5	W	
Aggregate Bit Rate	ABR	-	103.125	-	Gb/s	
Data Rate per Lane	DRL	-	25.78	-	Gb/s	
Control Input Voltage High	V_{IH}	$V_{CC} \cdot 0.7$	-	$V_{CC} + 0.3$	V	
Control Input Voltage Low	V_{IL}	-0.3	-	$V_{CC} \cdot 0.3$	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise	-	-	-	66	mVpp	10Hz -10MHz
Rx Differential Data Output Load	-	-	100	-	ohms	
Operating Distance	-	2	-	10,000	m	

Optical and Electrical Characteristics

Table 3 – Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	λ_{C0}	1264.5	1271	1277.5	nm	
Wavelength L1	λ_{C1}	1284.5	1291	1297.5	nm	
Wavelength L2	λ_{C2}	1304.5	1311	1317.5	nm	
Wavelength L3	λ_{C3}	1324.5	1331	1337.5	nm	
Side-mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Optical Launch Power	P_{OUT}	-	-	8.5	dBm	
Average launch power of OFF transmitter (Each Lane)	P_{OUT_OFF}	-	-	-30	dBm	
Average Optical Launch Power (Each Lane)	P_{OUTL}	-6.5	-	2.5	dBm	
Extinction Ratio	ER	3.5	-	-	dB	
Optical Modulation Amplitude (Each Lane)	OMA	-4	-	2.5	dBm	
Launch Power in OMA minus TDP (Each Lane)	OMA-TDP	-5	-	-	dBm	
Difference in launch power between any two lanes (Average and OMA)	P_{OUT_DIFF}	-	-	6	dB	
Transmitter and Dispersion Penalty (Each Lane)	TDP	-	-	3	dB	
Optical Return Loss Tolerance	ORLT	20	-	-	dB	
Transmitter Reflectance	TR	-	-	-20	dB	
Transmitter Eye Mask Definition	-	{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				

Table 4 – Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	λ_{C0}	1264.5	1271	1277.5	nm	
Wavelength L1	λ_{C1}	1284.5	1291	1297.5	nm	
Wavelength L2	λ_{C2}	1304.5	1311	1317.5	nm	
Wavelength L3	λ_{C3}	1324.5	1331	1337.5	nm	
Receiver Sensitivity (OMA) per Lane	-	-	-	-11.5	dBm	Note 1
Stressed Receiver Sensitivity in OMA (Each Lane)	-	-	-	-8.6	dBm	
Stressed Receiver Sensitivity Test Conditions:						
Stressed Eye J2 Jitter (Each Lane)	-	-	0.33	-	UI	
Stressed Eye J4 Jitter (Each Lane)	-	-	0.48	-	UI	
Vertical Eye Closure Penalty	-	-	2.6	-	dB	
Damage Threshold For Receiver	$P_{in, damage}$	3.5	-	-	dBm	
Average Receive Power (Each Lane)	-	-13	-	2.5	dBm	
Receive Power in OMA (Each Lane), Overload	OMA	-	-	2.5	dBm	
Receiver Reflectance	RX_R	-	-	-26	dB	

Note 1: Measured with conformance test signal at TP3 for BER = 5×10^{-5} .

Table 5 – Electrical Specifications
High-Speed Signal: Compliant to CAUI-4 (IEEE 802.3bm)

Low-Speed Signal: Compliant to SFF-8679

Transmitter (Module Input)						
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Differential Data Input Amplitude	$V_{IN,P-P}$	95	-	900	mVpp	Note 1
Differential Termination Mismatch		-	-	10	%	
LPMode, Reset and ModSelL	V_{IL}	-0.3	-	$V_{CC} \cdot 0.3$	V	
	V_{IH}	$V_{CC} \cdot 0.7$	-	$V_{CC} + 0.3$	V	
Receiver (Module Output)						
Differential Data Output Amplitude	$V_{OUT,P-P}$	250	-	900	mVpp	Note 1
Differential Termination Mismatch		-	-	10	%	
Output Rise/Fall Time, 20%~80%	T_R	9.5	-	-	ps	
ModPrsL and IntL	V_{OL}	0	-	0.4	V	$I_{OL}=4mA$
	V_{OH}	$V_{CC}-0.5$	-	$V_{CC}+0.3$	V	$I_{OL}=-4mA$

Note 1: Amplitude customization beyond these specs is dependent on validation in customer system

Timing

Table 6 – Timing for QSFP+ Soft Control and Status Functions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Initialization Time	t_init	-	-	2000	ms	
Reset Init Assert Time	t_reset_init	-	-	50	μs	Note 2
Serial Bus Hardware Ready Time	t_serial	-	-	2000	ms	
Monitor Data Ready Time	t_data	-	-	2000	ms	
Reset Assert Time	t_reset	-	-	2000	ms	
LPMode Assert Time	ton_LPMode	-	-	100	μs	
LPMode De-assert Time	toff_LPMode	-	-	300	ms	
IntL Assert Time	ton_IntL	-	-	200	ms	
IntL Deassert Time	toff_IntL	-	-	500	μs	
Rx LOS Assert Time	ton_lol	-	-	100	ms	
Tx Fault Assert Time	ton_Txfault	-	-	200	ms	
Flag Assert Time	ton_flag			200	ms	
Mask Assert Time	ton_mask			100	ms	
Mask Deassert Time	toff_mask			100	ms	
Application or Rate Select Change Time	t_ratesel			N/A	ms	Note 1
Power_over-ride or Power-set Assert Time	ton_Pdown			100	ms	
Power_over-ride or Power-set De-assert Time	toff_Pdown		-	300	ms	

Note 1: This feature is unsupported.

Note 2: A reset is generated by a low level longer than t_reset_init present on the ResetL input.

Table 7 – I/O Timing for Squelch & Disable

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq			80	μs	
Rx Squelch Deassert Time	toff_Rxsq			80	μs	
Tx Squelch Assert Time	ton_Txsq			400	ms	Note 1
Tx Squelch Deassert Time	toff_Txsq			400	ms	Note 1
Tx Disable Assert Time	ton_txdis			100	ms	
Tx Disable Deassert Time	toff_txdis			400	ms	
Rx Output Disable Assert Time	ton_rxdis			100	ms	
Rx Output Disable Deassert Time	toff_rxdis			100	ms	
Squelch Disable Assert Time	ton_sqdis			100	ms	
Squelch Disable Deassert Time	toff_sqdis			100	ms	

Note 1: Not implemented by default. This feature is configurable at factory.

Table 8 – Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V _{CC}	3%	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-6.5 to 2.5	±3	dB	Internal
Rx Power (Each Lane)	-13 to 2.5	±3	dB	Internal

Table 9 – Pin Definitions

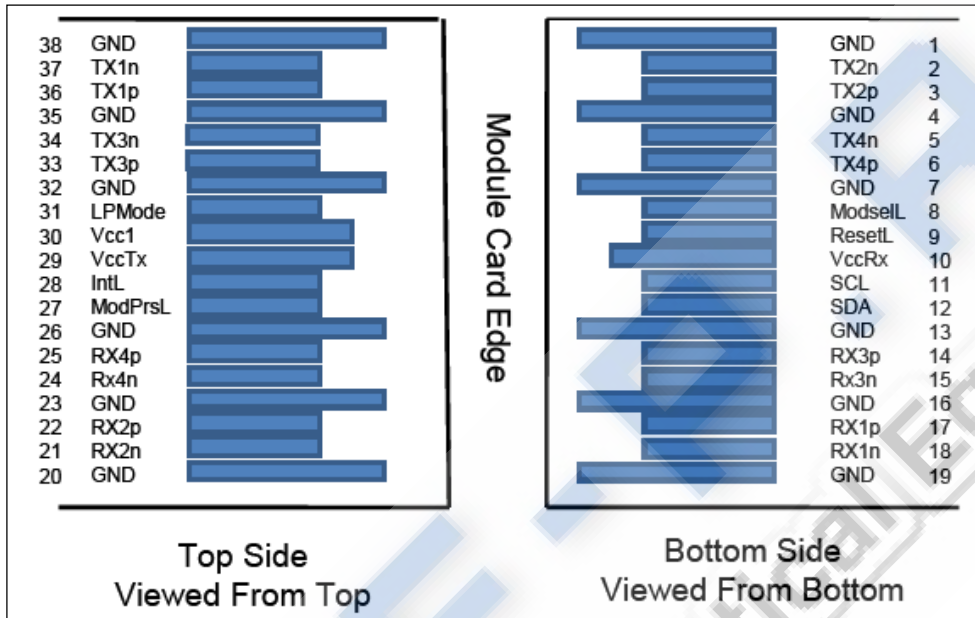
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModselL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted.

Connect these directly to the host board signal-common ground plane.

Note2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently.

QSFP+ Module Pad Layout



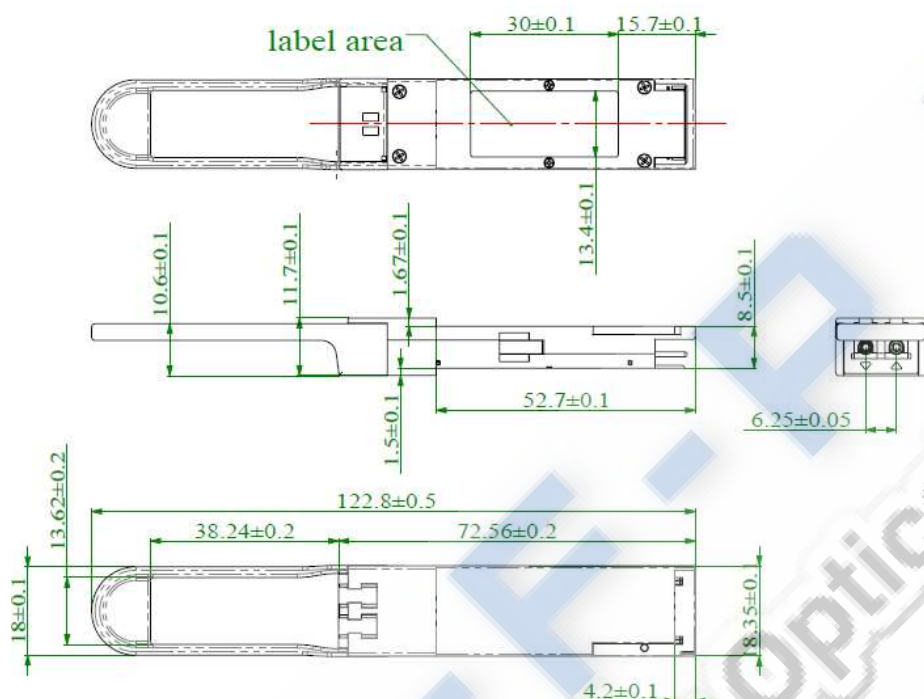
Recommended Host Board Power Supply Filtering

See SFF-8679

Recommended Boot-up Sequence:

1. Host asserts LPMODE input
2. Host powers up module and module will be held in low power mode
3. Host brings up PHY/MAC/PCS and makes sure RF signal is transmitted towards module
(Comment: RF signal can be offered anywhere during boot-up.)
4. Host de-asserts LPMODE input and the module will enter high power mode.
5. Host delay t_{init} (2s)
6. Host checks Initialization Complete Flag (byte 06 bit 0). After entering high power mode, this bit will be "1" and cleared after read. If no "1" is read, the boot-up has failed.
7. Host reads interrupt flags (A0.02-0E including Data_Not_Ready flag and all of the interrupt flags) to clear IntL output during initialization

Mechanical Diagram



Order Information

Table 10 – Order Information

Part No.	Application	Data Rate	Laser Source	Fiber Type
SPQ-CE-CL-CDFD	100G CWDM4	103.125 Gb/s	CWDM DML	SMF

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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