Finisar

Product Specification

10Gb/s 40km XFP Optical Transceiver

FTRX-1611-3

PRODUCT FEATURES

- Supports 9.95Gb/s to 10.7Gb/s bit rates
- Hot-pluggable XFP footprint
- Maximum link length of 40km
- Temperature-stabilized EML transmitter
- Duplex LC connector
- Power dissipation <3.5W
- Built-in digital diagnostic functions
- Temperature range: -5°C to 70°C

APPLICATIONS

- SONET OC-192 IR-2
  SDH STM S-64.2b
  SONET OC-192 IR-3
  SDH STM S-64.3b
  ITU-T G.709
- 10GBASE-ER/EW
  10GBASE-ER/EW + FEC
- 40km 10G Fibre Channel

Finisar's 40km FTRX-1611-3 Small Form Factor 10Gb/s (XFP) transceivers comply with the current XFP Multi-Source Agreement (MSA) Specification[1]. They comply with SONET OC-192 IR-2, OC-192 IR-3, SDH STM S-64.2b, STM S-64.3b as well as with 10-Gigabit Ethernet 10GBASE-ER/EW per IEEE 802.3ae and 40km 10G Fibre Channel applications. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA.

PRODUCT SELECTION

FTRX-1611-3

I. Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – **Not required**	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	
4	LVTTL-O	$\overline{\text{Interrupt}}$	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready; Finisar defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – **Not required**	
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – **Not required**	
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.

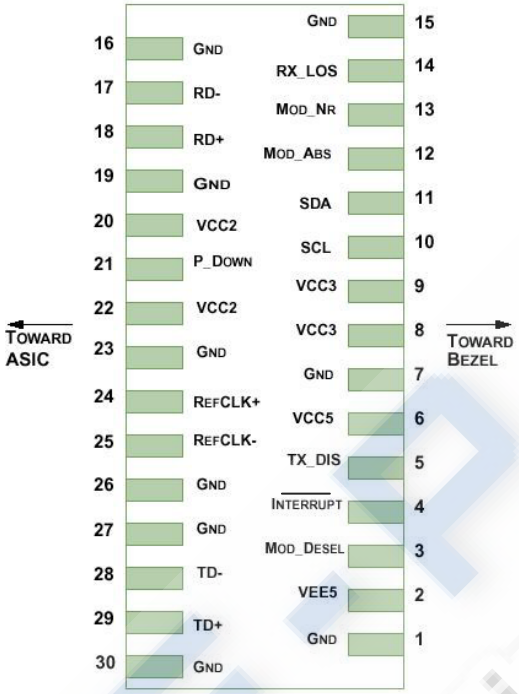


Diagram of Host Board Connector Block Pin Numbers and Names

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage 1	Vcc3	-0.5		4.0	V	
Maximum Supply Voltage 2	Vcc5	-0.5		6.0	V	
Storage Temperature	T_S	-40		85	°C	
Case Operating Temperature	T_{OP}	-5		70	°C	

III. Electrical Characteristics (T_{OP} = -5 to 70 °C, V_{CC5} = 4.75 to 5.25 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Main Supply Voltage	Vcc5	4.75		5.25	V	
Supply Voltage #2	Vcc3	3.13		3.45	V	
Supply Voltage #3	Vcc2	1.71		1.89	V	
Supply Current – Vcc5 supply	Icc5			350	mA	
Supply Current – Vcc3 supply	Icc3			400	mA	
Supply Current – Vcc2 supply	Icc2			750	mA	
Module total power	P			3.5	W	1
Transmitter						
Input differential impedance	R_{in}		100		Ω	2
Differential data input swing	Vin,pp	120		820	mV	
Transmit Disable Voltage	V_D	2.0		Vcc	V	3
Transmit Enable Voltage	V_{EN}	GND		GND+ 0.8	V	
Transmit Disable Assert Time				10	us	
Receiver						
Differential data output swing	Vout,pp	340	650	850	mV	4
Data output rise time	t_r			38	ps	5
Data output fall time	t_f			38	ps	5
LOS Fault	$V_{LOS\ fault}$	Vcc – 0.5		Vcc_{HOST}	V	6
LOS Normal	$V_{LOS\ norm}$	GND		GND+0.5	V	6
Power Supply Rejection	PSR	See Note 6 below				7
Reference Clock						
Clock differential input impedance	$Rclk_{in}$		100		Ω	
Reference Clock frequency	f0		Baud/64		MHz	
Differential clock input swing	Vclkin,pp	640		1600	mV	
Clock output rise/fall time	t_{rf}	200		1250	ps	5
Reference clock frequency tolerance	Df	-100		+100	PPM	

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. After internal AC coupling.
3. Or open circuit.
4. Into 100 ohms differential termination.
5. 20 – 80 %
6. Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
7. Per Section 2.7.1. in the XFP MSA Specification[1].

IV. Optical Characteristics (T_{OP} = -5 to 70°C, V_{CC5} = 4.75 to 5.25 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Output Opt. Pwr: 9/125 SMF	P_{OUT}	-1		+2	dBm	1
Optical Extinction Ratio	ER	8.2			dB	1
Center Wavelength	λc	1530		1565	nm	
Transmitter Dispersion Penalty (@ 800 ps/nm)	TDP			2	dB	
Sidemode Supression ratio	SSR_{min}	30			dB	
Tx Jitter Generation (peak-to-peak)	Tx_j			0.1	UI	2
Tx Jitter Generation (RMS)	Tx_{jRMS}			0.01	UI	3
Relative Intensity Noise	RIN			-130	dB/Hz	
Receiver						
Receiver Sensitivity @ 9.95Gb/s to 11.1Gb/s	R_{SENS1}			-16	dBm	4
Stressed Receiver Sensitivity (OMA) @ 10.3Gb/s	R_{SENS2}			-11.3	dBm	5
Maximum Input Power	P_{MAX}	-1			dBm	
Optical Center Wavelength	λ_C	1270		1600	nm	
Receiver Reflectance	R_{rx}			-27	dB	
Path penalty at 40km				2	dB	6
LOS De-Assert	LOS_D			-22	dBm	
LOS Assert	LOS_A	-28			dBm	
LOS Hysteresis		0.5			dB	

Notes:
1. Having ER=8.2dB guarantees that the –1 dBm minimum output power meets IEEE 802.3ae requirement of minimum OMA = -2.4 dBm.
2. Measured with a host jitter of 50 mUI peak-to-peak.
3. Measured with a host jitter of 7 mUI RMS.
4. Measured with worst ER; BER<10^{-12}; PRBS31. Equivalent to –14.3 dBm OMA at ER = 8.2 dB.
5. Per IEEE 802.3ae. Equivalent to –14.3 dBm average power at Infinite ER.
6. Dispersion penalty is measured in loopback using 18 ps/(nm*km) fiber (SMF-28).

V. General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Bit Rate	BR	9.95		10.7	Gb/s	1
Bit Error Ratio	BER			10^{-12}		2
Max. Supported Link Length	L_{MAX}		40		km	1

Notes:
1. SONET OC-192 IR-2, OC-192 IR-3, 10GBASE-ER/EW, 10G Fibre Channel, ITU-T G.709, 10GBASE-ER/EW + FEC
2. Tested with a $2^{31} - 1$ PRBS

VI. Environmental Specifications

Finisar XFP transceivers have an operating temperature range from -5°C to +70°C case temperature.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	-5		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

Finisar XFP transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard	Certificate Number
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50	9210176-60
Laser Eye Safety	TÜV	EN 60825-1: 1994+A11:1996+A2:2001 IEC 60825-1: 1993+A1:1997+A2:2001 IEC 60825-2: 2000, Edition 2	In Process
Electrical Safety	TÜV	EN 60950	In Process
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87	In Process

Copies of the referenced certificates are available at Finisar Corporation upon request.

VIII. Digital Diagnostics Functions

As defined by the XFP MSA[1], Finisar XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

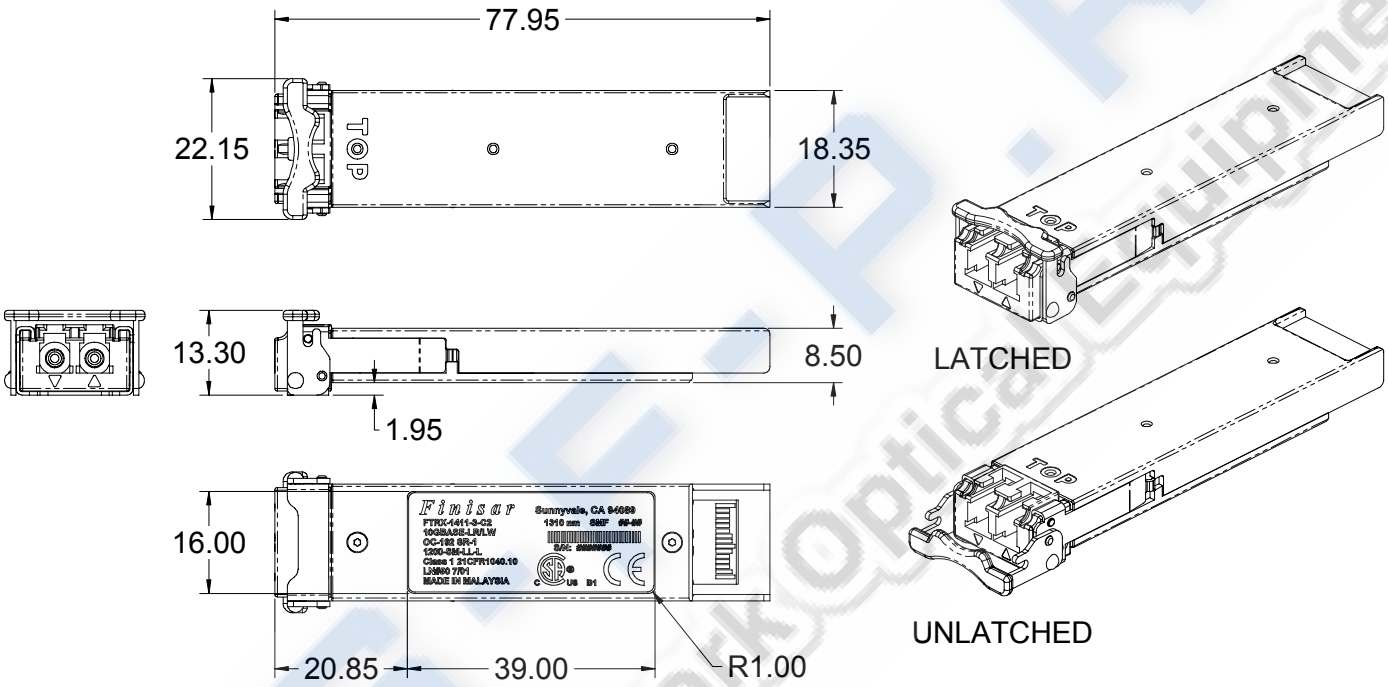
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information, including memory map definitions, please see the XFP MSA documentation[1].

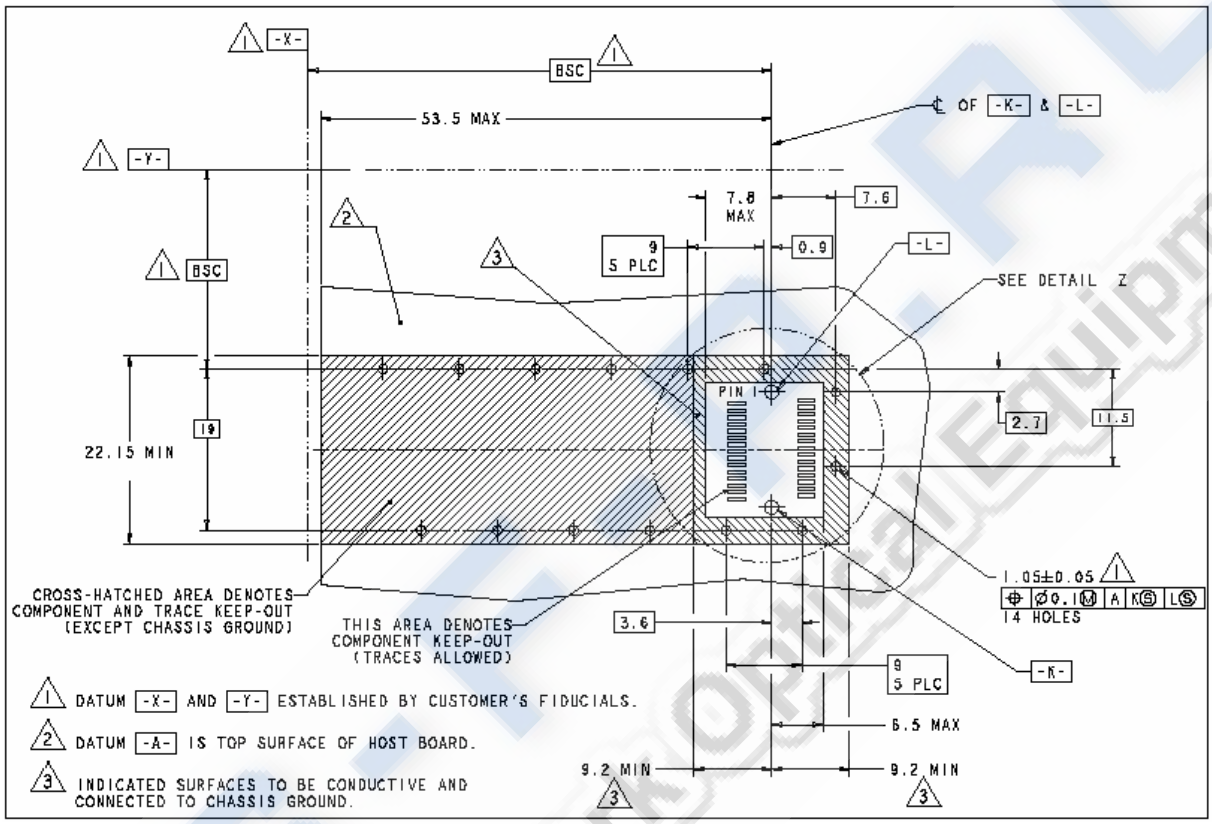
IX. Mechanical Specifications

Finisar's XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).

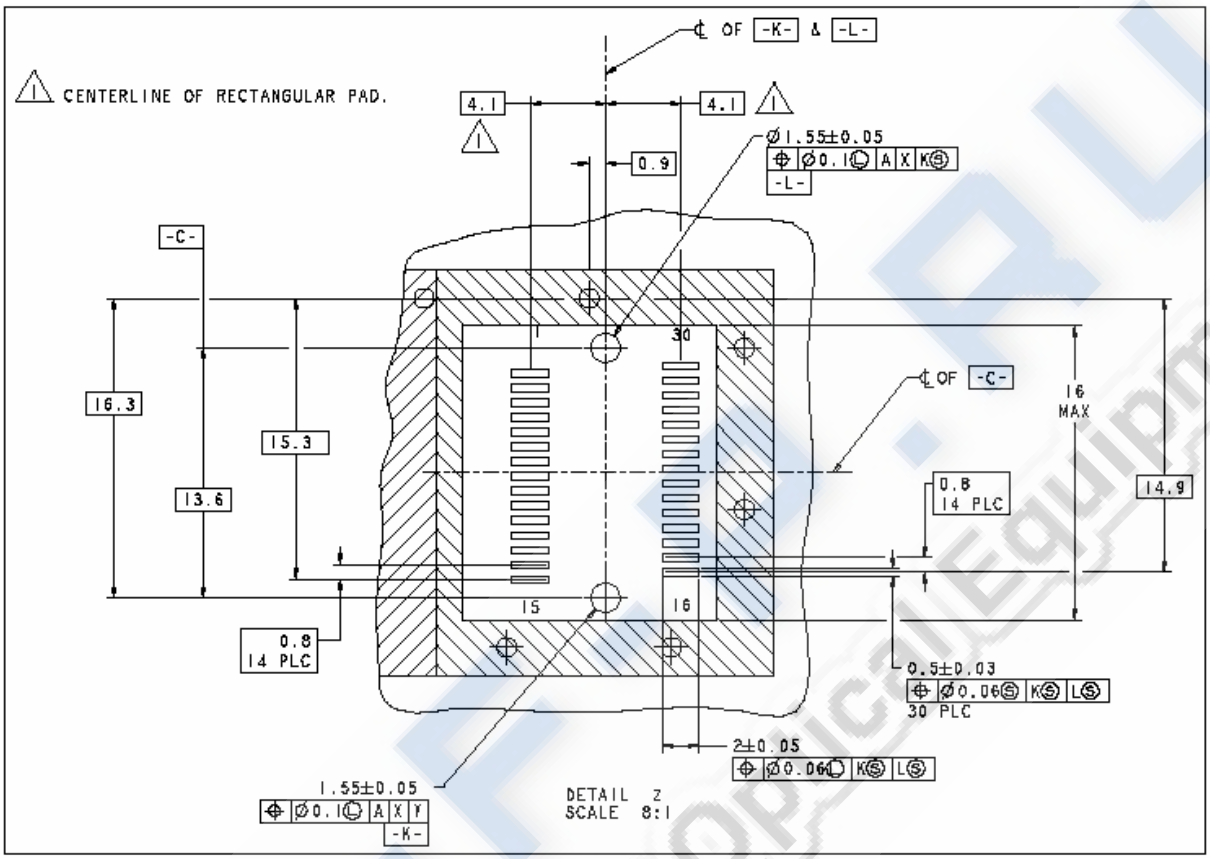


XFP Transceiver (dimensions are in mm)

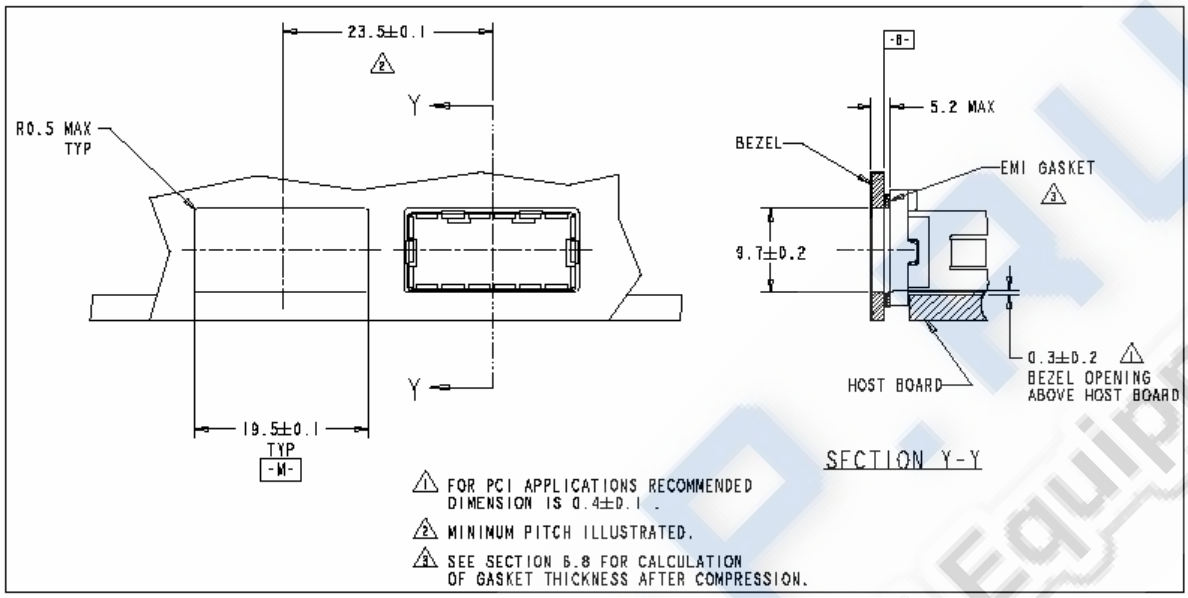
X. PCB Layout and Bezel Recommendations



XFP Host Board Mechanical Layout (dimensions are in mm)



XFP Detail Host Board Mechanical Layout (dimensions are in mm)



XFP Recommended Bezel Design (dimensions are in mm)

XI. References

1. 10 Gigabit Small Form Factor Pluggable Module (XFP) Multi-Source Agreement (MSA), Rev 4.0 - April 2004. Documentation is currently available at http://www.xfpmsa.org/

XII. For More Information

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