PRODUCT SPECIFICATION

Part No.:	AC-XFBL-23G10-10/AC-XFBL-32G10-10	
Description:	10G XFP Transceiver, BIDI TX1270nm/RX1330nm 10km 10G XFP Transceiver, BIDI TX1330nm/RX1270nm 10km	
Release Date	Rev.	Revision Change Description
2016/07/16	A0	New Release
2020/12/28	A1	Template Update

Features

- Supports 9.95Gbps to 11.3Gbps bit rates
- Hot-pluggable XFP footprint
- XFI Loopback Mode
- 1270nm DFB laser and PIN receiver for AC-XFBL-23G10-10
- 1330nm DFB laser and PIN receiver for AC-XFBL-32G10-10
- Up to10km for SMF transmission
- Compliant with XFP MSA with single LC receptacle
- Compatible with RoHS
- Single +3.3V power supply
- Power dissipation<2.0W
- 2-wire interface with integrated Digital Diagnostic monitoring
- EEPROM with Serial ID Functionality
- Operating case temperature:
- Standard: 0 to +70°C
- Industrial: -40 to +85°C

Application

- 10GBASE-BX 10.3125Gb/s Ethernet
- 10GBASE-BX 9.953Gb/s Ethernet
- SONET OC-192 SR-1 SDH STM I-64.1

Standard

- Compliant with SFF-8472
- Compliant with XFP MSA

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Specification:

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	0	4	V
Storage Temperature	Ts	-40	+85	℃
Operating Humidity	-	5	95	%
Signal Input Voltage		Vcc-0.3	Vcc+0.3	V

Recommended Operating Conditions

Parameter		Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Standard	Tc	0		+70	℃
	Industrial		-40		+85	℃
Power Supply Voltage		Vcc	3.135	3.30	3.465	V
Power Supply Current		Icc			600	mA
Data Rate				10.3	11.3	Gbps
Fiber Length 9/125μm core SMF			-	10	-	km

Optical and Electrical Characteristics

Parameter		Symbol	Min	Typical	Max	Unit	Notes
Transmitter							
Centre Wavelength		λc	1260	1270	1280	nm	AC-XFBL-23G10-10
			1320	1330	1340	nm	AC-XFBL-32G10-10
Spectral Width（-20dB）		Δλ			1	nm	
Side-Mode Suppression Ratio		SMSR	30	-		dB	
Average Output Power		P_{out}	-5		0	dBm	1
Extinction Ratio		ER	3.5			dB	
Data Input Swing Differential		V_{IN}	120		820	mV	2
Input Differential Impedance		Z_{IN}	85	100	115	Ω	
TX Disable	Disable		2.4		Vcc	V	
	Enable		-0.3		0.8	V	
TX Fault	Fault		2.0		Vcc+0.3	V	

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	Normal		-0.3		0.8	V	
Receiver							
Centre Wavelength		λc	1320	1330	1340	nm	AC-XFBL-23G10-10
			1260	1270	1280	nm	AC-XFBL-32G10-10
Receiver Sensitivity					-15	dBm	3
Receiver Overload			0.5			dBm	3
LOS De-Assert		LOS_D			-17	dBm	
LOS Assert		LOS_A	-32			dBm	
LOS Hysteresis			0.5		4	dB	
Data Output Rise/Fall time		tr/tf		20		ps	
LOS Output Voltage-High		VLOSH	2		Vcc	V	
LOS Output Voltage-Low		VLOSL	-0.3		0.4	V	
Receiver LOS Pull up Resistor		RLOS	4.7		10	KOhm	

Notes:

1. The optical power is launched into SMF.
2. PECL input, internally AC-coupled and terminated.
3. Measured with a $PRBS2^{31}$-1 test pattern @10312Mbps, BER ≤1×10^{-12}.

Digital Diagnostic Memory Map

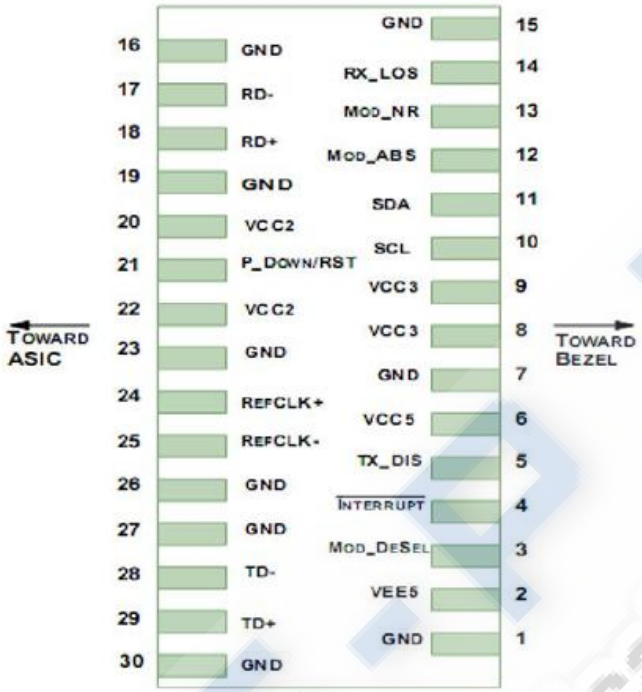
AC-XFBL-23/32G10-10 As defined by the XFP MSA, XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.For more detailed information including memory map definitions, please see the XFP MSA Specification.

Pin Descriptions



Pin Assignment

Pin	Signal Name	Description	Plug Seq.	Notes
1	GND	Module Ground		1
2	VEE5	Optional –5.2 Power Supply – Not required		
3	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	LVTTL-I	
4	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	LVTTL-O	2
5	TX_DIS	Transmitter Disable; Transmitter laser source turned off	LVTTL-I	
6	VCC5	+5 Power Supply		
7	GND	Module Ground		1
8	VCC3	+3.3V Power Supply		
9	VCC3	+3.3V Power Supply		
10	SCL	Serial 2-wire interface clock	LVTTL-I	2
11	SDA	Serial 2-wire interface data line	LVTTL-I/O	2
12	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	LVTTL-I	2
13	Mod_NR	Module Not Ready; XGIGA defines it as a logical OR	LVTTL-I	2

		between RX_LOS and Loss of Lock in TX/RX.		
14	RX_LOS	Receiver Loss of Signal indicator	LVTTL-I	2
15	GND	Module Ground		1
16	GND	Module Ground		1
17	RD-	Receiver inverted data output	CML-O	
18	RD+	Receiver non-inverted data output	CML-O	
19	GND	Module Ground		1
20	VCC2	+1.8V Power Supply – Not required		
21	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset Reset; The falling edge initiates a complete reset of the module	LVTTL-I	
22	VCC2	including the 2-wire serial interface, equivalent to a power cycle. +1.8V Power Supply – Not required		
23	GND	Module Ground		1
24	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	PECL-I	3
25	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	PECL-I	3
26	GND	Module Ground		1
27	GND	Module Ground		1
28	TD-	Transmitter inverted data input	CML-I	
29	TD+	Transmitter non-inverted data input	CML-I	
30	GND	Module Ground		1

Notes:

Plug Seq.: Pin engagement sequence during hot plugging.

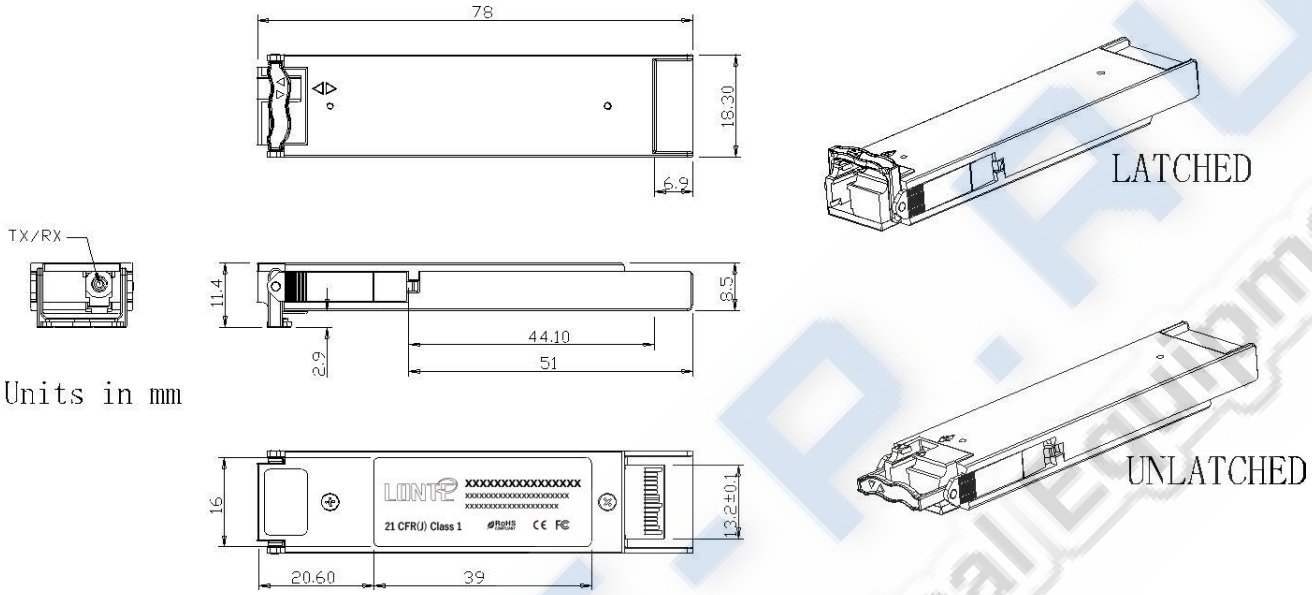
1) Module circuit ground is isolated from module chassis ground within the module.

2) Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.

3) A Reference Clock input is not required by the AC-XFBL-23/32G10-10. If present, it will be ignored.

Package Outline

Dimensions are in millimeters. All dimensions are ±0.2mm unless otherwise specified. (Unit: mm)



Regulatory Compliance

Feature	Test	Method
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>1000V for SFI pins, >2000Vfor other pins.)
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2	Class 2(>4.0kV)
Electromagnetic Interference (EMI)	CISPR22 ITE Class B FCC Class B CENELEC EN55022 VCCI Class 1	Comply with standard
Immunity	IEC61000-4-3	Comply with standard
Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Compatible with Class I laser Product

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Ordering information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX (nm)	Sen (dBm)	Temp (℃)	Reach (km)	DDM
AC-XFBL-23G10-10	XFP	10.3125	1270	-5~0	1330	<-15	0~70	10	Y
AC-XFBL-32G10-10	XFP	10.3125	1330	-5~0	1270	<-15	0~70	10	Y
AC-XFBL-23G10-10F	XFP	10.3125	1270	-5~0	1330	<-15	-40~85	10	Y
AC-XFBL-32G10-10F	XFP	10.3125	1330	-5~0	1270	<-15	-40~85	10	Y

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